CLAIMS:

1. An electric device (1, 100) with a body (2, 101) having:

- a resistor (36, 250) comprising a phase change material which is able to be in a first phase and in a second phase, the resistor (36, 250) having a surface with a first contact area (5, 132) and a second contact area (6, 272), the resistor (36, 250) having an electrical resistance between the first contact area (5, 132) and the second contact area (6, 272), the electrical resistance having a first value when the phase change material is in the first phase and a second value when the phase change material is in the second phase,
- a first conductor (3, 130) electrically connected to the first contact area (5, 132),
- a second conductor (4, 270) electrically connected to the second contact area (6, 272),
- the first conductor (3, 130), the second conductor (4, 270) and the resistor (36, 250) being able to conduct a current for heating of the phase change material to enable a transition from the first phase to the second phase, and
- a layer (20, 39, 126, 140, 260) of a dielectric material for reducing a heat flow to parts of the body (2, 101) free of the resistor (36, 250) during the heating, the dielectric material comprising a porous material with pores having a size between 0.5 and 50 nm.

2. An electric device (1, 100) as claimed in claim 1, wherein the pores have a size between 1 and 10 nm.

3. An electric device (1, 100) as claimed in claim 1, wherein the pores are substantially free of water.

4. An electric device (1, 100) as claimed in claim 1, wherein the pores have hydrophobic surfaces.

5. An electric device (1, 100) as claimed in claim 4, wherein the porous material comprises an organosilicate and the hydrophobic surfaces have hydrocarbyl groups.

6. An electric device (1, 100) as claimed in claim 5, wherein the porous material is obtainable by

- applying a liquid layer of a composition comprising tetra-alkoxysilane, hydrocarbylalkoxysilane, a surfactant and a solvent onto a substrate, wherein the molar ratio between tetra-alkoxysilane and hydrocarbylalkoxysilane is 3:1 at the most, and
- heating the liquid layer to remove the surfactant and the solvent and to form the hydrophobic porous layer.

7. An electric device (1, 100) as claimed in claim 6, characterized in that the surfactant is a cationic surfactant, and the surfactant and the totality of alkoxysilanes are present in a molar ratio greater than 0.1:1.

8. An electric device (1, 100) as claimed in claim 1, characterized in that the porous material has a porosity above 20 percent.

9. An electric device (1, 100) as claimed in claim 1, characterized in that the resistor (36, 250) is embedded in the body (2, 101), the layer (39, 126, 140, 260) being in direct contact with the resistor (36, 250).

10. An electric device (100) as claimed in claim 9, characterized in that the first contact area (132) is smaller than the second contact area (272), and the first conductor (130) comprises a part in direct contact with the first contact area (132), the part being embedded in the layer (126, 140).

11. An electric device (1, 100) as claimed in claim 1, characterized in that the first conductor (3, 130), the second conductor (4, 270), the resistor (36, 250) and the layer (20, 39, 126, 140, 260) constitute a memory element (30, 103), and the body (2, 101) comprises:

- an array of memory cells, each memory cell comprising a respective memory element (30, 103) and a respective selection device (26, 104), and
- a grid of select lines (12, 42, 120, 190),

each memory cell being individually accessible via the respective select lines (12, 42, 120, 190) connected to the respective selection device (26, 104).

12. An electric device (100) as claimed in claim 11, characterized in that:

- the selection device (104) comprises a metal oxide semiconductor field effect transistor having a source region (110), a drain region (112) and a gate region (116), and
- the grid of select lines comprises N first select lines (190), M second select lines (120), N and M being integers, and an output line (271),

the first conductor (130) of each memory element (103) being electrically connected to a first region selected from the source region (110) and the drain region (112) of the corresponding metal oxide semiconductor field effect transistor, the second conductor (270) of each memory element (103) being electrically connected to the output line (271), a second region of the corresponding metal oxide semiconductor field effect transistor which is selected from the source region (110) and the drain region (112) and which is free from the first region, being electrically connected to one of the N first select lines (190), the gate region (116) being electrically connected to one of the M second select lines (120).